ABSTRACT

The present invention relates to a semiconductor memory device. A voltage generator for supplying a sense amplifier I/O voltage (VSIO) and a voltage generator for supplying a bit line precharge voltage (VBLP) are independently separated. It is possible to prevent the bit line precharge voltage (VBLP) from increasing when the sense amplifier I/O voltage (VSIO) is increased due to the introduction of a column reset voltage (VCORE).